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2001, now U.S. Patent No. 6,385,075, granted May 7, 2002, entitled "Parallel Access of Cross-Point Diode Memory Arrays," the disclosures of which are hereby incorporated herein by reference.

The Abstract on page 22, as follows:

ABSTRACT OF THE DISCLOSURE

An electrical marking device is disposed on at least one layer of a data storage array having multiple layers of data storage medium. The marking device comprises at least one display layer that may be visually altered to display information, such as the nature, subject matter, and content of the data and amount of memory storage used. The display layer comprises a plurality of data storage cells, wherein the visual appearance of each of the data storage cells is varied depending on the value of the data bit. A method is also provided for electrically marking the content of an electrical data storage device having a storage array unit with multiple layers of data storage medium. Data is stored on an outermost layer of the data storage array to electrically provide a visual display indicating information about the stored data.

In the Claims:

1. (amended) An electrically addressable device for recording, addressing and reading of data, comprising:

a storage array unit having multiple layers of data storage medium, each of said layers being mounted on a substrate; and

an electrical marking device associated with at least one of the layers of storage medium of the storage array unit to provide a display indicating pre-selected information.

- 3. (amended) The electrically addressable device as recited in claim 2, wherein the display layer further comprises a plurality of multiple-state information storage cells each representing a value of at least one data bit, wherein the visual appearance of each information storage cell varies depending on the state of the information storage cell.
- 4. (amended) The electrically addressable device as recited in claim 1, wherein the information storage cells each further comprises a multiple state electrical device which changes states depending on a value of the data bit and having variable visual appearance depending on the state of the electrical device.
- 7. (amended) The electrically addressable device as recited in claim 2, wherein the display layer comprises an outermost layer of the storage array unit.

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9. (amended) The electrically addressable device as recited in claim 7, and further comprising a reflective layer between the display layer and a next layer in the storage array unit.

K 10 20. (amended) The electrically addressable device as recited in claim 18, wherein the display indicates information about the nature of the content of data stored on the storage array unit.